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IS 9414-1-1 (1979): Detail specification for digital integrated circuits, Part 1: Nand gate, TTL, Section 1: Single, 8 input, positive [LITD 5: Semiconductor and Other Electronic Components and Devices]

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IS : 9414 (Part I/Sec 1) - 1979

(Reaffirmed 2006)

Indian Standard

DETAIL SPECIFICATION FOR DIGITAL INTEGRATED CIRCUITS

PART I NAND GATE, TTL

Section 1 Single, 8 Input, Positive

Semiconductor Devices and Integrated Circuits Sectional Committee, LTDC 10; Panel for Integrated Circuits, LTDC 10/P 6 [Ref : Doc : LTDC 10 (74)]

1. Scope — Covers two types of NAND gates based on their operating temperature range and other electrical characteristics (Type 1* and Type 2†).

1.1 Refer to IS : 7441 (Part I)-1974 'Essential ratings and characteristics of digital integrated circuits: Part I General format'.

1.2 The assigned type number shall be prominently displayed on the device.

2. Description

Category of device	Digital combinatorial
Configuration	Transistor-transistor-logic (TTL)
Function	Positive NAND gate
Gates per package	One
Inputs per gate	8 Inputs
Outputs per gate	1 Output
Technology used	Bipolar
Constructional detail	Monolithic
Material	Silicon

3. Outlines and Connections

3.1 *Outlines and Encapsulation*

Type of Device	Outline	Encapsulation
Type 1	Under consideration	Ceramic
Type 2	IS : 5000 (OD 15) - 1973*	Ceramic or plastic

*Dimensions of semiconductor devices and integrated circuits: Device outline OD 15.

3.2 *Logic Diagram and Connections* — The logic diagram and pin connections shall be as shown in Fig. 1.

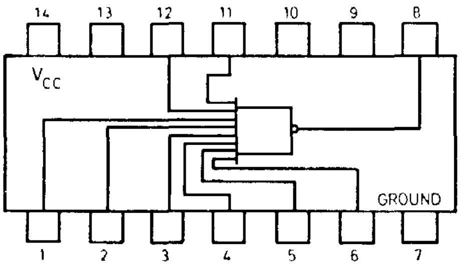

FIG. 1 PIN CONNECTIONS

4. Functional Specification

4.1 *Block Diagram* — The block diagram of a typical input NAND gate is shown in Fig. 2.

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*Type 1 corresponds to commercial type 5430.

†Type 2 corresponds to commercial type 7430.

Adopted 13 August 1979

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Gr 3

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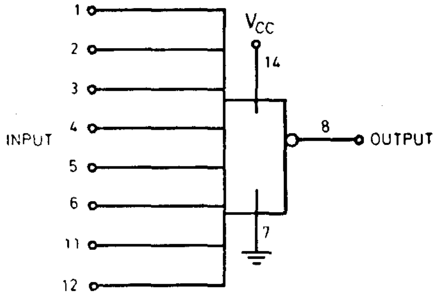

FIG. 2 BLOCK DIAGRAM

4.2 *Schematic Diagram (Each Gate)* — The schematic diagram of the gate is shown in Fig. 3.

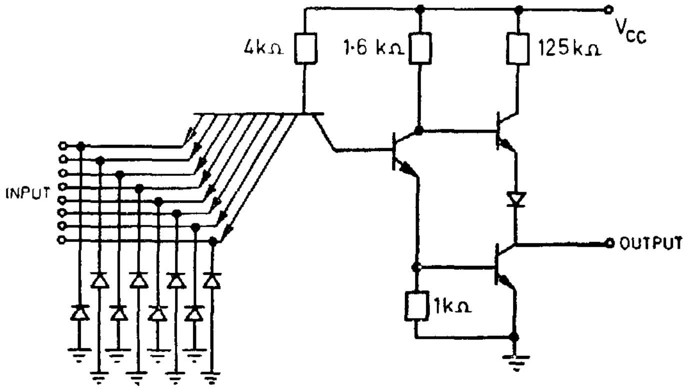

FIG. 3 SCHEMATIC DIAGRAM

Note — The components and values are given only as an example.

4.2.1 The details of the schematic diagram should always be specified or indicated by the manufacturer.

4.3 *Function* — *See* Table 1.

TABLE 1 FUNCTION

Input 1	Input 2	Input 3	Input 4	Input 5	Input 6	Input 7	Input 8	Output 9
(1)	(2)	(3)	(4)	(5)	(6)	(7)	(8)	(9)
H	*H*	*H*	*H*	*H*	*H*	*H*	*H*	*L*

Note — All other combinations of *H* and *L* at the input give *H* output.

H = High state, most positive (least negative).
L = Low state, least positive (most negative).

5. Ratings (Absolute Maximum)

5.1 *Electrical Ratings*

Rating	Value		Remarks
	Max	*Min*	
Supply voltage V_{CC}	+7·0 V	− 0·5 V	These voltages are with respect to ground terminal
Input voltage V_{IN}	+ 5·5 V	− 1·5 V (At high level input current I_{IH} of 12 mA *Max*)	

5.1.1 *Conditions for recommended operation*

a) Supply voltage

Type of Device	Supply Voltage V_{CC} Volts		
	Min	*Nom*	*Max*
Type 1	4·5	5·0	5·5
Type 2	4·75	5·0	5·25

b) Output loading capability (fan out), $N = 10$ *Max*

5.1.2 *DC noise margins*

$M_1 = V_{IHA} - V_{OHA}$ = Not applicable
$M_2 = V_{OHB} - V_{IHB}$ = 400 mV
$M_3 = V_{ILA} - V_{OLA}$ = 400 mV
$M_4 = V_{OLB} - V_{ILB}$ = Not applicable

Note — For explanation of the symbols given above, reference to **10.1** of IS : 7441 (Part I) - 1974 may be made.

5.2 *Temperature Ratings*

a) *Operating temperature*

Type 1	−55°C to +125°C
Type 2	−0°C to +70°C

b) *Storage temperature*

Type 1 Type 2	−65°C to +150°C

c) *Junction temperature*

Type 1 Type 2	175°C

d) *Thermal resistance (junction to case)*

Type 1	0·03°C/mW
Type 2	0·08°C/mW

5.3 *Power Dissipation (Typical)*

Type 1	40 mW/gate at 50 percent duty cycle
Type 2	10 mW/gate at 50 percent duty cycle

5.4 *Marking* — Refer to IS : 9596 'General requirements and classification of tests for micro-circuits'.

6. Electrical Characteristics

6.1 Electrical characteristics shall be as specified in Table 2. The values specified apply over the full operating temperature range [*see* **5.2**(a)].

TABLE 2 ELECTRICAL CHARACTERISTICS

(*Clause* 6.1)

Characteristics	Symbol	Clause No. of IS : 9501 (Part I)-1980*	Condition	Limit		Remarks
				Min	*Max*	
(1)	(2)	(3)	(4)	(5)	(6)	(7)
a) Functional Tests						
i) Verification of type of micro-circuit	—	4	—	—	—	—
b) *Static Tests*						
i) High level output	V_{OH}	10	†V_{CC} = *min* I_{OH} = −400 µA V_{IL} = 0·8 V	2·4 V	—	*See* Note 1
ii) Low level output voltage	V_{OL}	9	†V_{CC} = *min* V_{IH} = 2V for all inputs of gate under test	—	—	*See* Note 2
iii) Input clamp voltage	V_I	—	I_{OL} = 16 mA †V_{CC} = *min* I_H = −12 mA	—	1·5 V	—
iv) High level input voltage	V_{IH}	—	†V_{CC} = *min*	2·0	—	—
v) Low level input voltage	V_{IL}	—	†V_{CC} = *min*	—	0·8	—
vi) High level input current (each input)	I_{IH}	8	†V_{CC} = *max* V_{IH} = 2·4 V	—	40 µA	*See* Note 2
vii) High level input current (each input)	I_{IH}	8	†V_{CC} = *max* V_{IH} = 5·5 V	—	1mA (for Type 1) and 100 µA (for Type 2)	*See* Note 2
viii) Low level input current (each input)	I_{IL}	7	†V_{CC} = *max* V_{IL} = 0·4 V	−0·7 mA —	1·6 mA for Type 1 1·6 mA for Type 2	
ix) Short circuit output current	I_{OS}	14	†V_{CC} = *max*	−20 mA	−55 mA	*See* Notes 2 and 3
x) High level supply current per gate	I_{CCH}	13	V_{IL} = OV †V_{CC} = *max*	—	1·65 mA	*See* Note 1
xi) Low level supply current per gate	I_{CCL}	13	†V_{CC} = *max* V_{IH} = 5·5	—	5 mA	*See* Note 2
c) *Switching Tests*						
Type 1, At 25°C V_{CC} = *nom*						
i) Propagation delay time, high-to-low level	t_{PHL}	21 22	C_L = 50 pF R_L = 390Ω	3 ns	20 ns	—
ii) Propagation delay time, low-to-high	t_{PLH}	21 22	C_L = 50 pF R_L = 390Ω	3 ns	25 ns	—
Type 1 at −55°C and +125°C and V_{CC} = *nom*						
iii) Propagation delay time, high-to-low level	t_{PHL}	21 22	C_L = 50 pF R_L = 390Ω	3 ns	24 ns	—
iv) Propagation delay time, low-to-high level	t_{PLH}	21 22	C_L = 50 pF R_L = 390Ω	3 ns	27 ns	—
Type 2 at 25°C, V_{CC} = *nom*						
v) Propagation delay time, high-to-low level	t_{PHL}	21 22	C_L = 15 pF R_L = 390Ω	—	15 ns	—
vi) Propagation delay time, low-to-high level	t_{PLH}	21 22	C_L = 15 pF R_L = 390Ω	—	22 ns	—

Note 1 — All unspecified inputs at V_{CC} = *max*.

Note 2 — All unspecified inputs grounded.

Note 3 — Not more than one output should be shorted at a time.

*Methods of measurement of electrical characteristics of micro-circuits: Part I Digital micro-circuits.

†For value of V_{CC} reference should be made to **5.1**(a).

7. Environmental Data

	Type 1	*Type 2*
a) Temperature severity (cold/ dry heat)	55°C/125°C	0°C/70°C
b) Damp heat	Composite temperature/humidity cyclic	Not Applicable
c) Shock	15 km/s^2	15 km/s^2
d) Acceleration (steady state)	200 km/s^2	200 km/s^2
e) Vibration	20 *g*, 20-2 000 Hz, 6 hours	20 *g*, 20-2 000 Hz, 6 hours

8. Tests

8.1 The provisions for type approved procedure and batch acceptance procedure as given in IS : 9596 shall apply.

8.2 The test schedule and requirements shall be as given in Table 3.

TABLE 3 TEST SCHEDULE AND REQUIREMENTS

(*Clause* 8.2)

Sl No.	No. of Specimens	Test	Clause of IS : 9597 (Part I)*	Condition of Test and Requirements	Remarks†
(1)	(2)	(3)	(4)	(5)	(6)
a) *Group 0*					
i)	All	Visual Examination	23	—	Type 1 and Type 2
ii)	All	Initial Measurements: 1) Static tests 2) Switching tests	—	*See* Table 2	,,
b) *Group 1*					
i)	5 or as applicable	Physical dimensions	13	—	Type 1 and Type 2
ii)	,,	Marking permanency	15	—	,,
iii)	,,	Solderability	18	—	,,
c) *Group 2*					
i)	5 or as applicable	Robustness of termination	16	Lead fatigue	,,
ii)	,,	Sealing	17	Fine leak Gross leak	Type 1 Type 1
iii)	,,	Final Measurements: 1) Static tests 2) Switching tests	—	*See* Table 2	Type 1 and Type 2
d) *Group 3*					
i)	5 or as applicable	Impact (shock)	9	15 km/s^2	,,
ii)	,,	Vibration	22	20 *g*, 20-2 000 Hz, 6 h	,,
iii)	,,	Acceleration steady-state	1	200 km/s^2	,,
iv)	,,	Final measurements: 1) Static tests 2) Switching tests	—	*See* Table 2	,,
e) *Group 4*					
i)	5 or as applicable	Thermal shock	21	−55°C/125°C	Type 1
ii)	,,	Change of temperature	19	−65°C/155°C	Type 1 and Type 2
iii)	,,	Damp heat (cyclic)	6	6 cycles, 16 hours	Type 2
iv)	,,	Final Measurements: 1) Static tests 2) Switching tests	—	*See* Table 2	Type 1 and Type 2
f) *Group 5*					
i)	5 or as applicable	Corrosive atmosphere (salt mist)	5	—	Type 1
g) *Group 6*					
i)	5 or as applicable	Life (high temperature, non-operating)	12	—	Type 1 and Type 2
ii)	,,	Final Measurements: 1) Static tests 2) Switching tests	---	*See* Table 2	,,
h) *Group 7*					
i)	5 or as applicable	Life (steady state operation)	12	—	,,
ii)	,,	Final Measurements: 1) Static tests 2) Switching tests	—	*See* Table 2	,,

*General requirements and environmental and life tests for integrated circuits: Part I Environmental tests.

†This column specifies the type of device to which the test concerned is applicable.

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